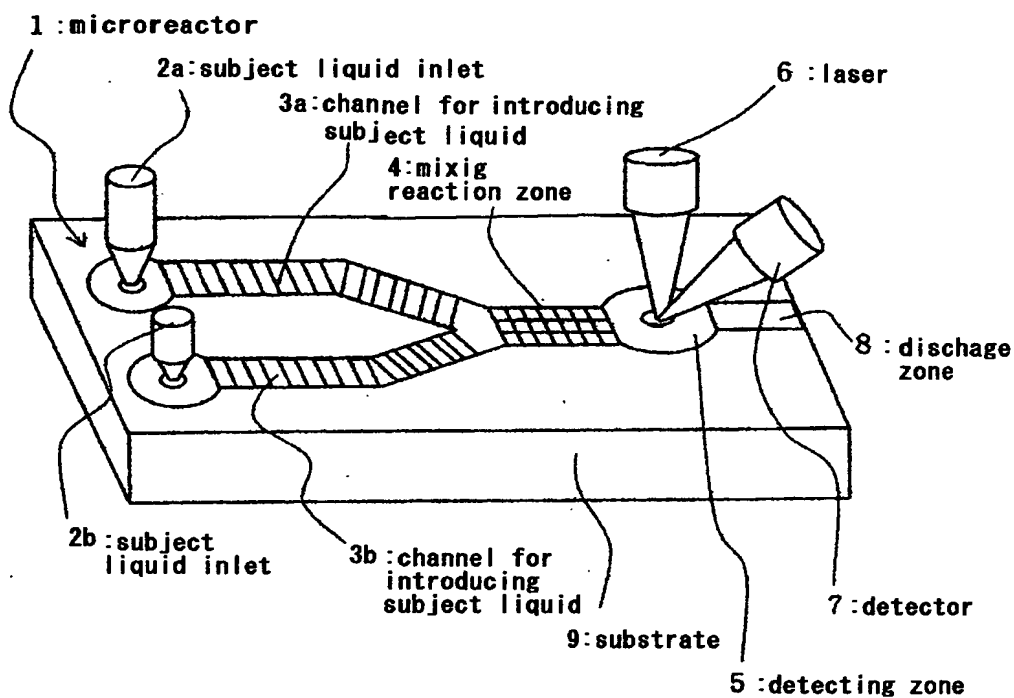


**Fig. 1**



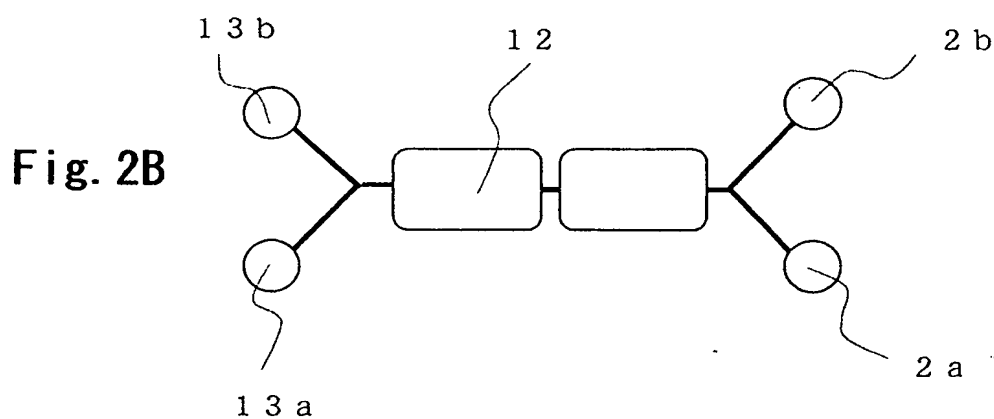
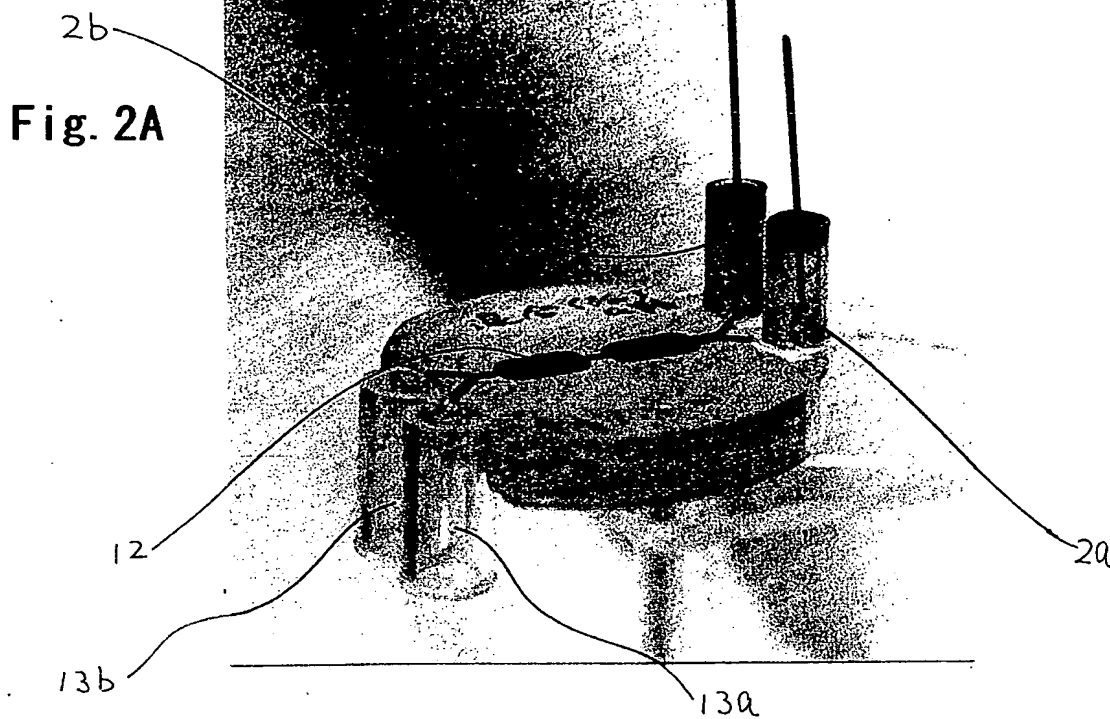


Fig. 3A

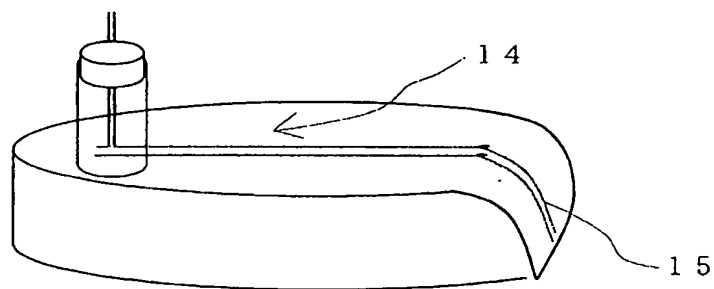


Fig. 3B

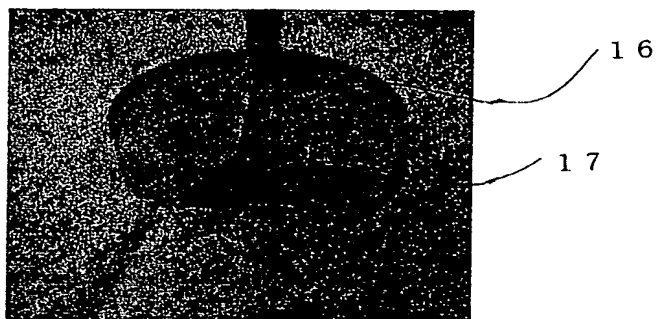


Fig. 3C

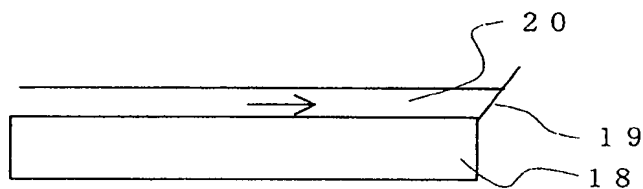
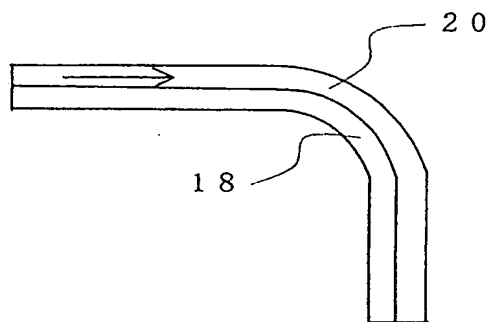
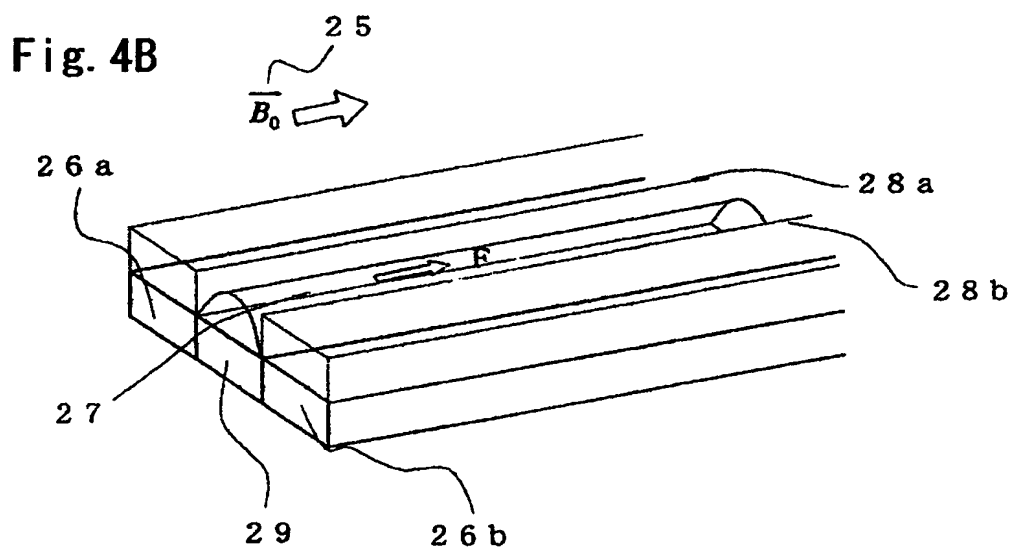
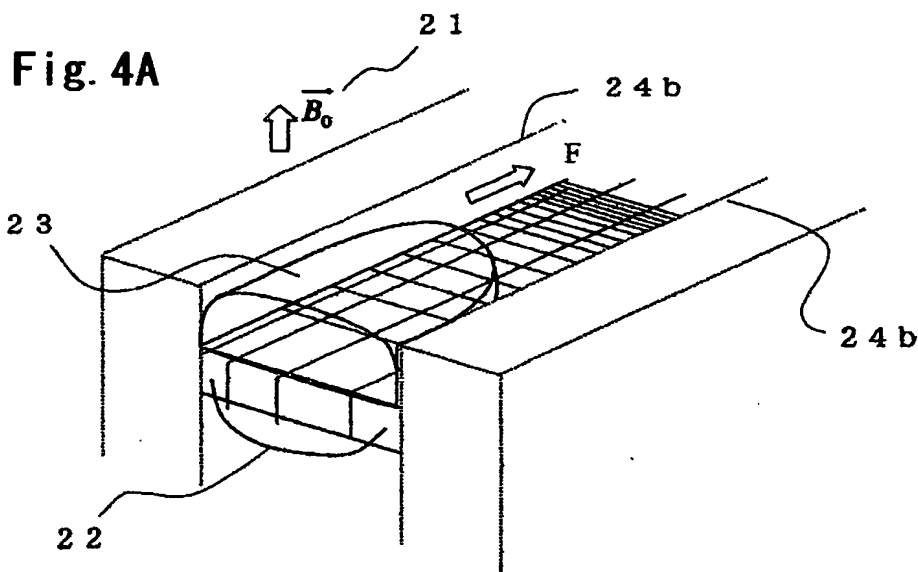


Fig. 3D





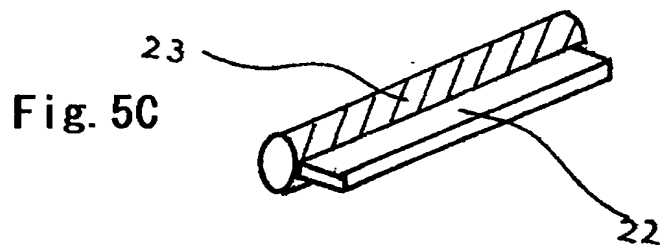
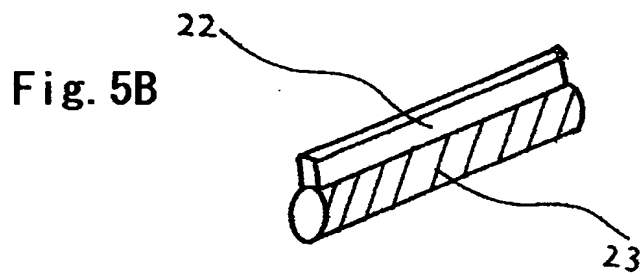
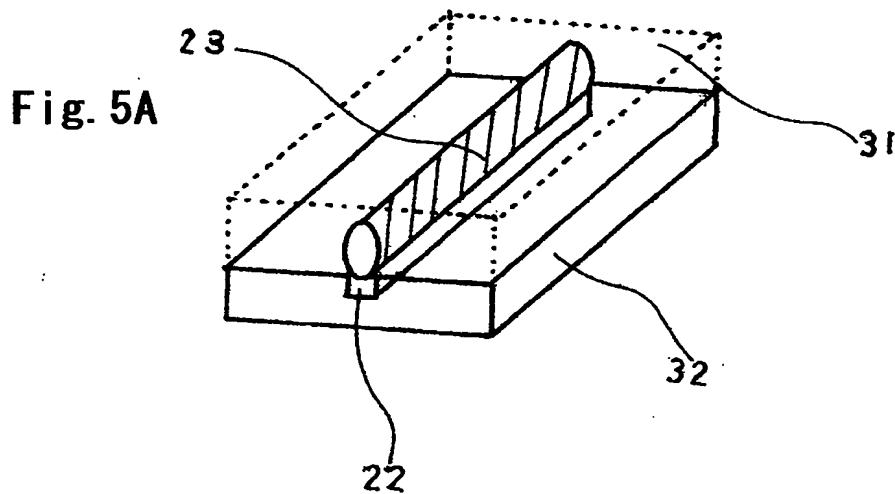


Fig. 6A



Fig. 6B



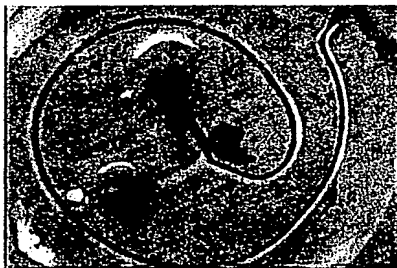
Fig. 7A



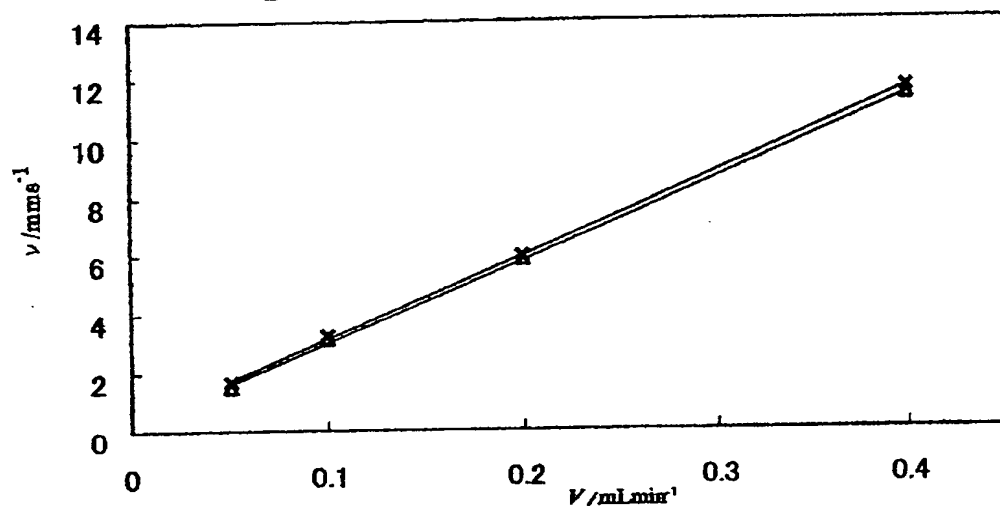
Fig. 7B



Fig. 7C



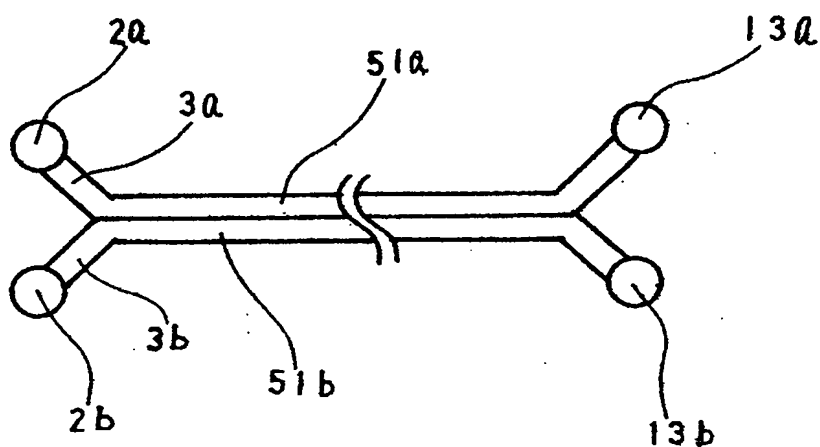
**Fig. 8**



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**Fig. 9**



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Fig. 10A

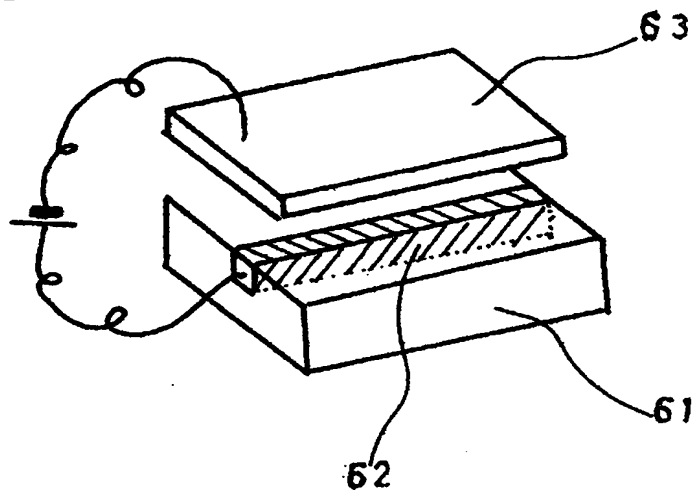


Fig. 10B

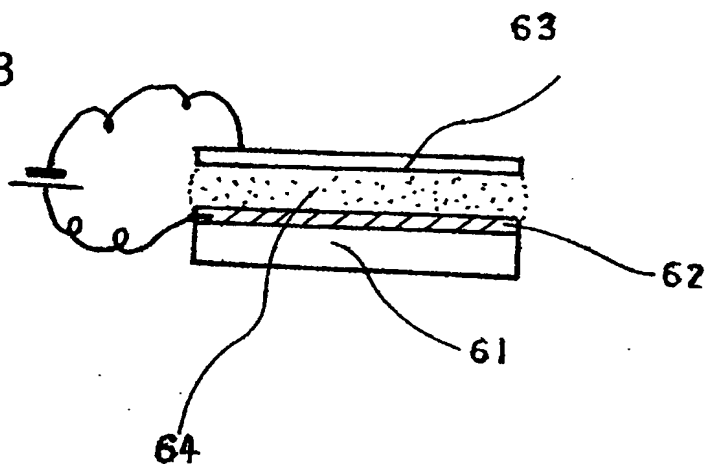


Fig. 11

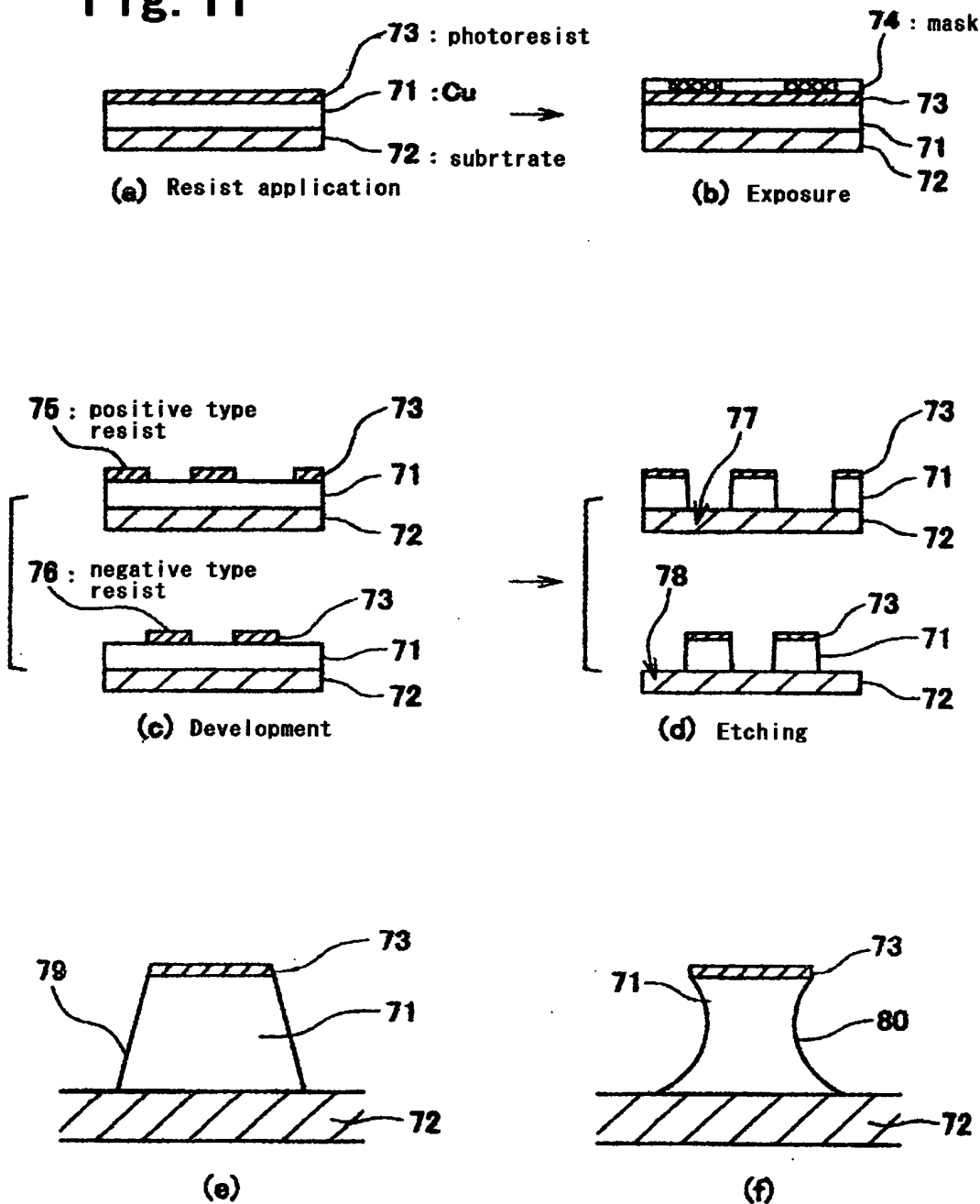
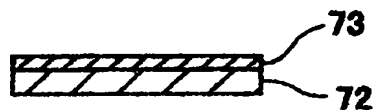
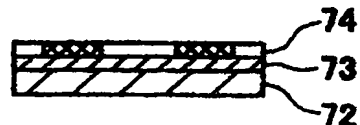


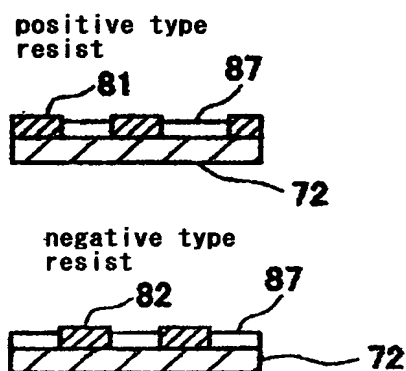
Fig. 12



(a) Resist application



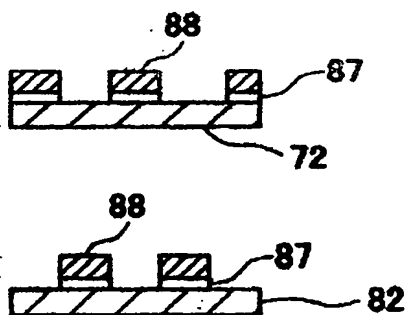
(b) Exposure



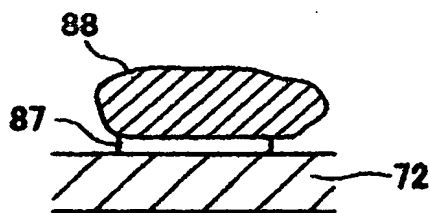
(c) Electroless plating after development



(d) Elimination of resist



(e) Thickening of circuit membrane by electroplating



(f) Magnified view

Fig. 13

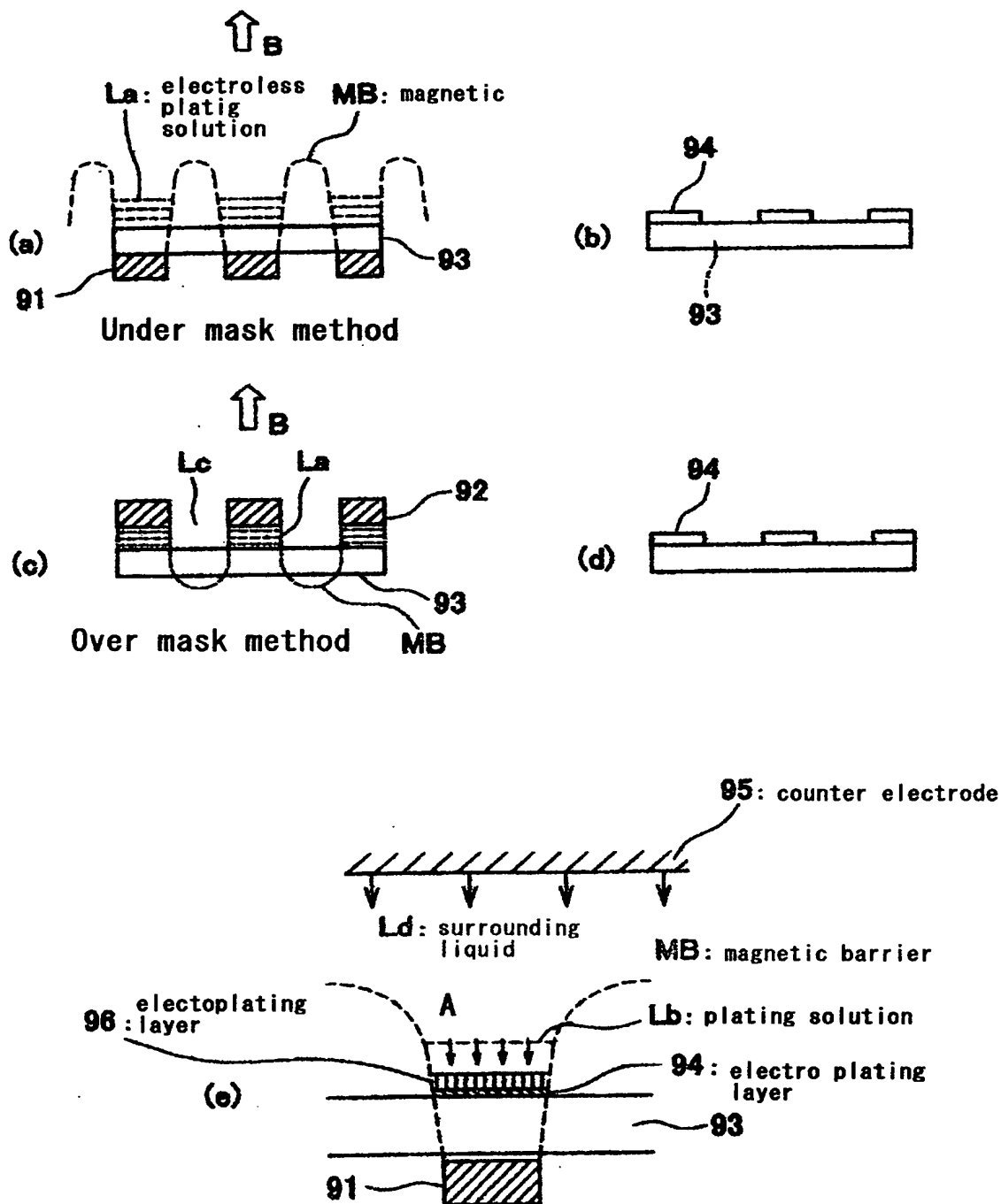
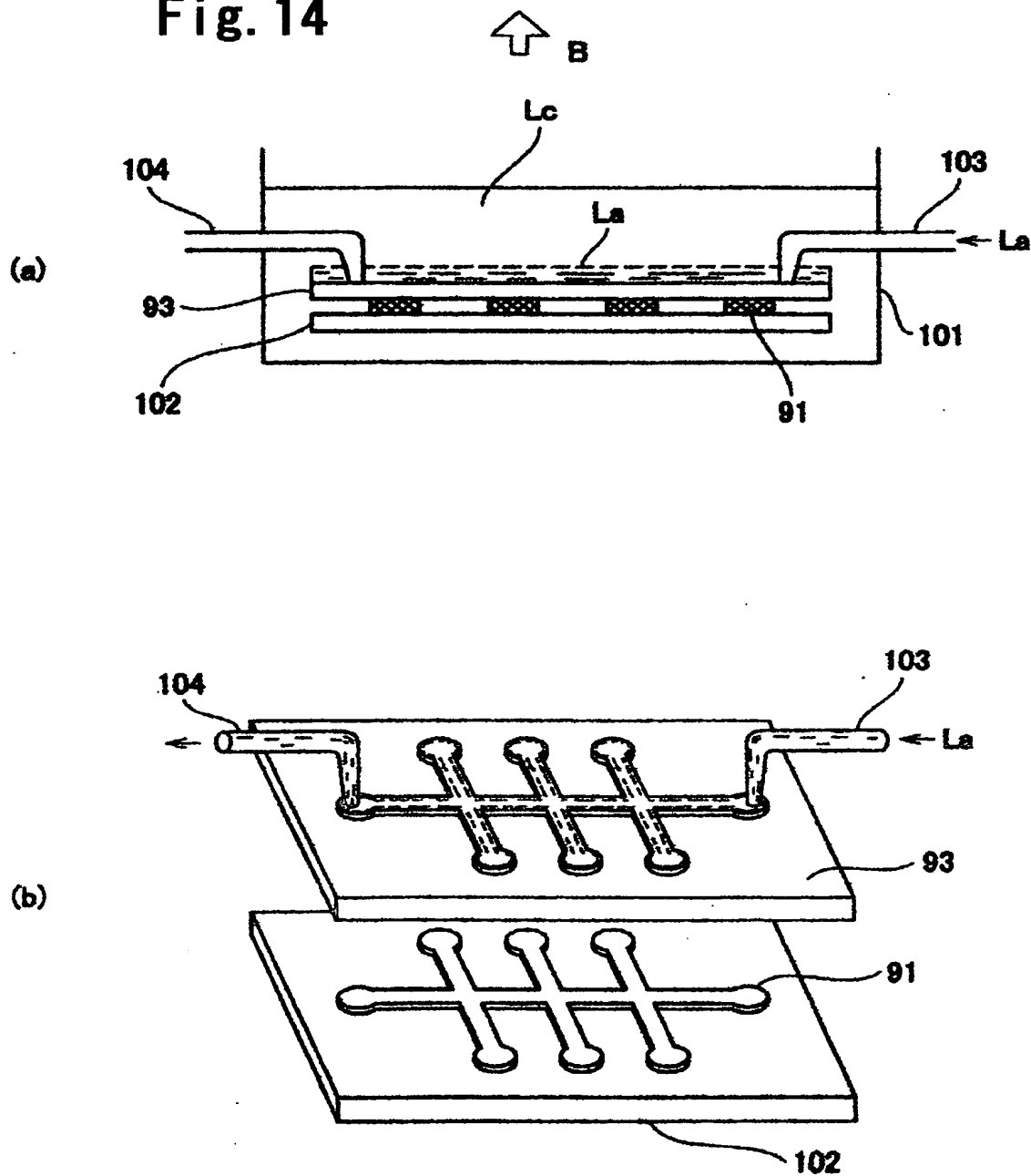
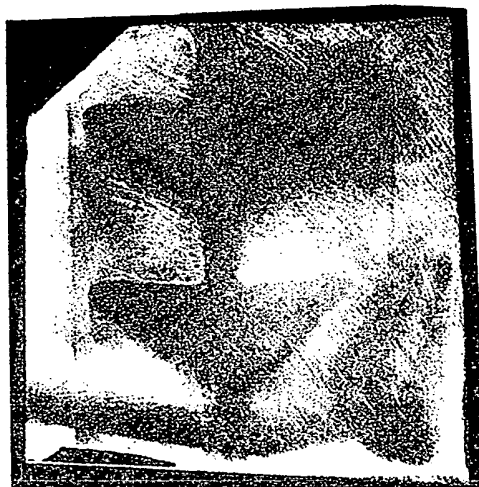


Fig. 14





**Fig. 16**



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